**EXPERIMENT 07:** SPICE Simulation of and implementation for JFET characteristics

**AIM:** Simulate output and transfer I-V characteristics for n-channel and p-channel JFET in common source configuration.

**SOFTWARE TOOL:** PC loaded with LT-Spice

**THEORY:**

**PART A**

**Introduction to LTspice:**

LTspice is freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology (LTC).

LTspice IV provides a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. Supplied with LTspice IV are macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components.

LTspice IV is node-unlimited and third-party models can be imported. Circuit simulations based on transient, AC, noise and DC analysis can be plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated.

LTspice IV is used within LTC, and by many users in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not generate printed circuit board (PCB) layouts, but netlists can be imported into layout programs. LTspice IV can't simulate a complex digital logic.

**PART B**

**Introduction to SPICE programming:**

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behaviour.

SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral-charge model of Gummel and Poon; however, if the Gummel- Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges. Different MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi-empirical model.

**Semiconductor Devices**

#### Junction Field Effect Transistors (JFET's)

 General form:

 JXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS,VGS>

 Examples:

 J1 7 2 3 JM1 OFF

ND, NG, and NS are the drain, gate, and source nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

#### JFET Models (both N and P Channel)

The JFET model is derived from the FET model of Shichman and Hodges. The dc characteristics are defined by the parameters VTO and BETA, which determine the variation of drain current with gate voltage, LAMBDA, which determines the output conductance, and IS, the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. Charge storage is modeled by nonlinear depletion layer capacitances for both gate junctions which vary as the -1/2 power of junction voltage and are defined by the parameters CGS, CGD, and PB.

 name parameter units default example

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 1 VTO threshold voltage V -2.0 -2.0

 2 BETA transconductance parameter A/V\*\*2 1.0E-4 1.0E-3

 3 LAMBDA channel length modulation

 parameter 1/V 0 1.0E-4

 4 RD drain ohmic resistance Ohm 0 100

 5 RS source ohmic resistance Ohm 0 100

 6 CGS zero-bias G-S junction capacitance F 0 5PF

 7 CGD zero-bias G-D junction capacitance F 0 1PF

 8 PB gate junction potential V 1 0.6

 9 IS gate junction saturation current A 1.0E-14 1.0E-14

10 FC coefficient for forward-bias - 0.5

 depletion capacitance formula

**PROBLEM STATEMENT 1A**

Simulate I-V transfer and output characteristics for an N-channel JFET in common source configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 1A**

**CIRCUIT SCHEMATIC will come here**

**Add separate circuits for output and transfer**

**PROBLEM STATEMENT 1B**

Simulate I-V transfer and output characteristics for an N-channel JFET in common source configuration using SPICE programming in LTspice

**SPICE CODE 1B**

**spice code for I-V transfer and output characteristics for an N-channel JFET**

**Write two separate spices codes for transfer and output curves**

**SIMULATION RESULT 1A and 1B**

**Simulation results for n-channel JFET transfer and output curve will come here**

**2 plots have to be attached here**

**Observe the following from the simulation plot for Problem Statement 1a and 1b**

1. **IDSS : \_\_\_\_\_\_\_\_**
2. **VP : \_\_\_\_\_\_\_\_**
3. **gm : \_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 2A**

Simulate I-V transfer and output characteristics for a P-channel JFET in common source configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 2A**

**CIRCUIT SCHEMATIC will come here**

**Take separate circuits for output and transfer**

**PROBLEM STATEMENT 2B**

Simulate I-V transfer and output characteristics for a P-channel JFET in common source configuration using SPICE programming in LTspice

**SPICE CODE 2B**

**spice code for I-V transfer and output characteristics for an P-channel JFET**

**Write two separate spices codes for transfer and output curves**

**SIMULATION RESULT 2A and 2B**

**Simulation results for p-channel JFET transfer and output curve will come here**

**2 plots have to be attached here**

**Observe the following from the simulation plot for Problem Statement 2a and 2b**

1. **IDSS : \_\_\_\_\_\_\_\_**
2. **VP : \_\_\_\_\_\_\_\_**
3. **gm : \_\_\_\_\_\_\_\_**

**CONLUSION:**