**EXPERIMENT NO. 06**

**AIM:** Simulate input and output I-V characteristics for npn BJT and pnp BJT in common emitter configuration and npn BJT in common base configuration.

**SOFTWARE TOOL:** PC loaded with LT-Spice

**THEORY:**

**PART A**

**Introduction to LTspice:**

LTspice is freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology (LTC).

LTspice IV provides a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. Supplied with LTspice IV are macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components.

LTspice IV is node-unlimited and third-party models can be imported. Circuit simulations based on transient, AC, noise and DC analysis can be plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated.

LTspice IV is used within LTC, and by many users in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not generate printed circuit board (PCB) layouts, but netlists can be imported into layout programs. LTspice IV can't simulate a complex digital logic.

**PART B**

**Introduction to SPICE programming:**

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources , switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral-charge model of Gummel and Poon; however, if the Gummel- Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges. Different MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi-empirical model.

**Semiconductor Devices**

#### Bipolar Junction Transistors (BJT's)

 General form:

 QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE,VCE>

 Examples:

 Q50A 11 26 4 20 MOD1

 Q23 10 24 13 QMOD IC=0.6,5.0

NC, NB, and NE are the collector, base, and emitter nodes, respectively. NS is the (optional) substrate node. If unspecified, ground is used. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

#### BJT Models (both NPN and PNP)

The bipolar junction transistor model in SPICE is an adaptation of the integral charge control model of Gummel and Poon. This modified Gummel-Poon model extends the original model to include several effects at high bias levels. The model will automatically simplify to the simpler Ebers-Moll model when certain parameters are not specified.

The dc model is defined by the parameters IS, BF and NE which determine the forward current gain characteristics, IS, BR and NC which determine the reverse current gain characteristics, and VAF and VAR which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC, and RE are included, where RB can be high current dependent. Base charge storage is modeled by forward and reverse transit times, TF and TR, the forward transit time TF being bias dependent if desired, and nonlinear depletion layer capacitances which are determined by CJE and VJE for the B-E junction , CJC and VJC for the B-C junction and CJS and VJS for the C-S (Collector-Substrate) junction. The BJT parameters used in the modified Gummel-Poon model are listed below.

 Modified Gummel-Poon BJT Parameters.

 name parameter units default example

 ---- --------- ----- ------- -

1 IS transport saturation current A 1.0E-16 1.0E-15

2 BF ideal maximum forward beta - 100 100

3 VAF forward Early voltage V infinite 200

4 ISE B-E leakage saturation current A 0 1.0E-13

5 NE B-E leakage emission coefficient - 1.5 2

6 BR ideal maximum reverse beta - 1 0.1

7 VAR reverse Early voltage V infinite 200

8 ISC B-C leakage saturation current A 0 1.0E-13

9 NC B-C leakage emission coefficient - 2 1.5

10 RB zero bias base resistance Ohms 0 100

11 RE emitter resistance Ohms 0 1

12 RC collector resistance Ohms 0 10

13 CJE B-E zero-bias depletion capacitance F 0 2PF

14 VJE B-E built-in potential V 0.75 0.6

15 TF ideal forward transit time sec 0 0.1Ns

16 CJC B-C zero-bias depletion capacitance F 0 2PF

17 VJC B-C built-in potential V 0.75 0.5

18 TR ideal reverse transit time sec 0 10Ns

19 CJS zero-bias collector-substrate

 capacitance F 0 2PF

20 VJS substrate junction built-in potential V 0.75

**PROBLEM STATEMENT 1A**

Simulate I-V input and output characteristics for a npn BJT (BC547B) in common emitter configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 1A**

**SAMPLE CIRCUIT SCHEMATIC**

**This is the sreen shot of the schematic.**

**Strickly take the circuit capture as as shown here**



****

**SIMULATION RESULT 1A**

**SAMPLE SIMULATION RESULTS**

**This is the sreen shot of the simulation results**

**Strickly take the result plot as as shown here**

****

****

**Observe the following on the simulation plot for Problem Statement 1a**

1. **Small-Signal Current Gain:**\_\_\_\_\_\_\_\_\_\_\_
2. **Dynamic input resistance: \_\_\_\_\_\_\_\_\_\_\_\_**
3. **Dynamic output resistance: \_\_\_\_\_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 1B**

Simulate I-V input and output characteristics for a npn BJT in common emitter configurations using SPICE programming in LTspice

**SPICE CODE 1B**

**SAMPLE spice code**

\*NPN BJT CE output characteristics

vbb 1 0 dc

rb 1 2 100k

q1 3 2 0 mybjt

rc 3 4 1k

vcc 4 0 dc

.model mybjt npn

.dc vcc 0 10 0.1 vbb 0.5 1 0.1

## Add model parameters like ( BF, VAF , CJE, CJC) in the above spice code and observe the changes in plots

For example:

.model mybjt npn ( BF=100, VAF=100, CJE=2pf, CJC=10pf)

\*NPN BJT CE input characteristics

vbb 1 0 dc

rb 1 2 100k

q1 3 2 0 mybjt

rc 3 4 1k

vcc 4 0 dc

.model mybjt npn

.dc vbb 0 2 0.1 vcc 2 6 2

## Add model parameters like ( BF, VAF , CJE, CJC) in the above spice code and observe the changes in plots

For example:

.model mybjt npn ( BF=100, VAF=100, CJE=2pf, CJC=10pf)

**SIMULATION RESULT 1B**

**Simulation results for npn BJT input and output curve will come here**

**4 plots have to be attached here (2 plots with no model parameters and 2 plots with model parameters)**

**Observe the following on the simulation plot for Problem Statement 1b (only with model parameters cases)**

1. **Small-Signal Current Gain:**\_\_\_\_\_\_\_\_\_\_\_
2. **Dynamic input resistance: \_\_\_\_\_\_\_\_\_\_\_\_**
3. **Dynamic output resistance: \_\_\_\_\_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 2A**

Simulate I-V input and output characteristics for a pnp BJT (BC557B) in common emitter configurations using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 2A**

**SAMPLE CIRCUIT SCHEMATIC**

**This is the sreen shot of the schematic.**

**Strickly take the circuit capture as as shown here**



****

**SIMULATION RESULT 2A**

**SAMPLE SIMULATION RESULTS**

**This is the sreen shot of the simulation results**

**Strickly take the result plot as as shown here**

**
**

**Observe the following on the simulation plot for Problem Statement 2a**

1. **Small-Signal Current Gain:**\_\_\_\_\_\_\_\_\_\_\_
2. **Dynamic input resistance: \_\_\_\_\_\_\_\_\_\_\_\_**
3. **Dynamic output resistance: \_\_\_\_\_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 2B**

Simulate I-V input and output characteristics for a pnp BJT in common emitter configurations using SPICE programming in LTspice

**SPICE CODE 2B**

**Spice code for pnp with model parameters**

**SIMULATION RESULT 2B**

**Simulation results for pnp BJT input and output curve will come here**

**Observe the following on the simulation plot for Problem Statement 2b (only with model parameters cases)**

1. **Small-Signal Current Gain:**\_\_\_\_\_\_\_\_\_\_\_
2. **Dynamic input resistance: \_\_\_\_\_\_\_\_\_\_\_\_**
3. **Dynamic output resistance: \_\_\_\_\_\_\_\_\_\_\_\_**

**PROBLEM STATEMENT 3A**

Simulate I-V input and output characteristics for a npn BJT (BC547B) in common base configuration using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 3A**

**SAMPLE CIRCUIT SCHEMATIC**

**This is the sreen shot of the schematic.**

**Strickly take the circuit capture as as shown here**

****

**SIMULATION RESULT 3A**

**Simulation for npn BJT in common base configurations will come here**

**PROBLEM STATEMENT 3B**

Simulate I-V input and output characteristics for a npn BJT in common base configuration using SPICE programming in LTspice

**SPICE CODE 3B**

**spice code for npn BJT in common base configurations will come here**

**SIMULATION RESULT 3B**

**Simulation results for npn BJT in common base configuration will come here**

**CONLUSION:**