**EXPERIMENT NO. 05**

**AIM:** Simulate I-V characteristics of pn and zener diode using LTspice

**SOFTWARE TOOL:** PC loaded with LT-Spice

**THEORY:**

**PART A**

**Introduction to LTspice :**

LTspice is freeware computer software implementing a SPICE simulator of electronic circuits, produced by semiconductor manufacturer Linear Technology (LTC).

LTspice IV provides a schematic capture and waveform viewer with enhancements and models to speed the simulation of switching regulators. Supplied with LTspice IV are macro models for 80% of LTC's switching regulators and operational amplifiers, transistors, MOSFETs, and passive components.

LTspice IV is node-unlimited and third-party models can be imported. Circuit simulations based on transient, AC, noise and DC analysis can be plotted as well as Fourier analysis. Heat dissipation of components can be calculated and efficiency reports can also be generated.

LTspice IV is used within LTC, and by many users in fields including radio frequency electronics, power electronics, digital electronics, and other disciplines. LTspice IV does not generate printed circuit board (PCB) layouts, but netlists can be imported into layout programs. LTspice IV can't simulate a complex digital logic.

**PART B**

**Introduction to SPICE programming :**

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

SPICE is a general-purpose circuit simulation program for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

SPICE has built-in models for the semiconductor devices, and the user need specify only the pertinent model parameter values. The model for the BJT is based on the integral-charge model of Gummel and Poon; however, if the Gummel- Poon parameters are not specified, the model reduces to the simpler Ebers-Moll model. In either case, charge-storage effects, ohmic resistances, and a current-dependent output conductance may be included. The diode model can be used for either junction diodes or Schottky barrier diodes. The JFET model is based on the FET model of Shichman and Hodges. Different MOSFET models are implemented: MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model, while MOS3 is a semi-empirical model;

**Types of analysis**

1. **DC analysis :** The dc analysis portion of SPICE determines the dc operating point of the circuit with inductors shorted and capacitors opened.

#### .DC statement

General form:

.DC SRCNAM VSTART VSTOP VINCR [SRC2 START2 STOP2 INCR2]

Examples:

.DC VIN 0.25 5.0 0.25

This card defines the dc transfer curve source and sweep limits. SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP, and VINCR are the starting, final, and incrementing values respectively. The first example will cause the value of the voltage source VIN to be swept from 0.25 Volts to 5.0 Volts in increments of 0.25 Volts.

1. **AC Small Signal Analysis :** The ac small-signal portion of SPICE computes the ac output variables as a function of frequency. The program first computes the dc operating point of the circuit and determines linearized, small-signal models for all of the nonlinear devices in the circuit. The resultant linear circuit is then analyzed over a user-specified range of frequencies.

#### .AC statement

General form:

.AC DEC ND FSTART FSTOP

.AC OCT NO FSTART FSTOP

.AC LIN NP FSTART FSTOP

Examples:

.AC DEC 10 1 10K

.AC DEC 10 1K 100MEG

.AC LIN 100 1 100HZ

DEC stands for decade variation, and ND is the number of points per decade. OCT stands for octave variation, and NO is the number of points per octave. LIN stands for linear variation, and NP is the number of points. FSTART is the starting frequency, and FSTOP is the final frequency. If this card is included in the deck, SPICE will perform an ac analysis of the circuit over the specified frequency range

1. **Transient Analysis :** The transient analysis portion of SPICE computes the transient output variables as a function of time over a user specified time interval. The initial conditions are automatically determined by a dc analysis. All sources which are not time dependent (for example, power supplies) are set to their dc value.

**.TRAN statement**

General form:

.TRAN TSTEP TSTOP <TSTART <TMAX>> <UIC>

Examples:

.TRAN 1NS 100NS

.TRAN 1NS 1000NS 500NS

.TRAN 10NS 1US UIC

TSTEP is the printing or plotting increment for line-printer output. For use with the post-processor, TSTEP is the suggested computing increment. TSTOP is the final time, and TSTART is the initial time. If TSTART is omitted, it is assumed to be zero. The transient analysis always begins at time zero. In the interval , the circuit is analyzed (to reach a steady state), but no outputs are stored. In the interval , the circuit is analyzed and outputs are stored. TMAX is the maximum step-size that SPICE will use (for default, the program chooses either TSTEP or (TSTOP-TSTART)/50.0, whichever is smaller. TMAX is useful when one wishes to guarantee a computing interval which is smaller than the printer increment, TSTEP.

**Circuit description**

The circuit to be analyzed is described to SPICE by a set of element lines, which define the circuit topology and element values, and a set of control lines, which define the model parameters and the run controls. The first line in the input file must be the title, and the last line must be ".END". The order of the remaining lines is arbitrary.

Each element in the circuit is specified by an element line that contains the element name, the circuit nodes to which the element is connected, and the values of the parameters that determine the electrical characteristics of the element. The first letter of the element name specifies the element type.

For example, a resistor name must begin with the letter R and can contain one or more characters. Hence, R, R1, RSE, ROUT, and R3A are valid resistor names.

Nodes names may be arbitrary character strings. The datum (ground) node must be named '0'.

Each node in the circuit must have a dc path to ground. Every node must have at least two connections.

**Element Description**

1. **Resistors**

General form:

RXXXXXXX N1 N2 VALUE <TC=TC1<,TC2>>

Examples:

R1 1 2 100

RC1 12 17 1K TC=0.001,0.015

N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and may be positive or negative but not zero.

#### Capacitors and Inductors

General form:

CXXXXXXX N+ N- VALUE <IC=INCOND>

LYYYYYYY N+ N- VALUE <IC=INCOND>

Examples:

CBYP 1 0 1UF

LLINK 42 69 1UH

N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads or the inductance in Henries.

#### Independent Sources

General form:

VXXXXXXX N+ N- <<DC> DC/TRAN VALUE> <AC <ACMAG <ACPHASE>>>

Examples:

VCC 10 0 DC 6

VIN 13 2 0.001 AC 1 SIN(0 1 1MEG)

N+ and N- are the positive and negative nodes, respectively. Note that voltage sources need not be grounded.

DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.

ACMAG is the ac magnitude and ACPHASE is the ac phase. The source is set to this value in the ac analysis. If ACMAG is omitted following the keyword AC, a value of unity is assumed. If ACPHASE is omitted, a value of zero is assumed. If the source is not an ac small-signal input, the keyword AC and the ac values are omitted.

**Semiconductor Devices**

#### Junction Diodes

General form:

DXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD>

Examples:

DBRIDGE 2 10 DIODE1

N+ and N- are the positive and negative nodes, respectively. MNAME is the model name, AREA is the area factor, and off indicates an (optional) starting condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

#### Bipolar Junction Transistors (BJT's)

General form:

QXXXXXXX NC NB NE <NS> MNAME <AREA> <OFF> <IC=VBE,VCE>

Examples:

Q50A 11 26 4 20 MOD1

Q23 10 24 13 QMOD IC=0.6,5.0

NC, NB, and NE are the collector, base, and emitter nodes, respectively. NS is the (optional) substrate node. If unspecified, ground is used. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

#### Junction Field Effect Transistors (JFET's)

General form:

JXXXXXXX ND NG NS MNAME <AREA> <OFF> <IC=VDS,VGS>

Examples:

J1 7 2 3 JM1 OFF

ND, NG, and NS are the drain, gate, and source nodes, respectively. MNAME is the model name, AREA is the area factor, and OFF indicates an (optional) initial condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed.

#### MOSFET's

General form:

MXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> <AD=VAL> <AS=VAL>+ <PD=VAL> <PS=VAL> <NRD=VAL> <NRS=VAL> <OFF> <IC=VDS,VGS,VBS>

Examples:

M1 24 2 0 20 TYPE1

M31 2 17 6 10 MODM L=5U W=2U

M31 2 16 6 10 MODM 5U 2U

M1 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U

M1 2 9 3 0 MOD1 10U 5U 2P 2P

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in meters. AD and AS are the areas of the drain and source diffusions, in sq-meters. Note that the suffix U specifies microns (1E-6 m) and P sq-microns (1E-12 sq-m). If any of L, W, AD, or AS are not specified, default values are used. The user may specify the values to be used for these default parameters on the .OPTIONS card. The use of defaults simplifies input deck preparation, as well as the editing required if device geometries are to be changed. PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the .MODEL card for an accurate representation of the parasitic series drain and source resistance of each transistor. PD and PS default to 0.0 while NRD and NRS to 1.0.

**.MODEL Statement**

General form:

.MODEL MNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ... )

Examples:

.MODEL MOD1 NPN BF=50 IS=1E-13 VBF=50

The .MODEL card specifies a set of model parameters that will be used by one or more devices. MNAME is the model name, and type is one of the following seven types:

NPN NPN BJT model

PNP PNP BJT model

D diode model

NJF N-channel JFET model

PJF P-channel JFET model

NMOS N-channel MOSFET model

PMOS P-channel MOSFET model

Parameter values are defined by appending the parameter name, as given below for each model type, followed by an equal sign and the parameter value. Model parameters that are not given a value are assigned the default values given below for each model type.

#### Diode Model

The dc characteristics of the diode are determined by the parameters IS and N. An ohmic resistance, RS, is included. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance which is determined by the parameters CJO, VJ, and M. The temperature dependence of the saturation current is defined by the parameters EG, the energy and XTI, the saturation current temperature exponent. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV (both of which are positive numbers).

name parameter units default example

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1 IS saturation current A 1.0E-14 1.0E-14

2 RS ohmic resistance Ohm 0 10

3 N emission coefficient - 1 1.0

4 TT transit-time sec 0 0.1Ns

5 CJO zero-bias junction capacitance F 0 2PF

6 VJ junction potential V 1 0.6

7 M grading coefficient - 0.5 0.5

8 EG activation energy eV 1.11 1.11 Si

0.69 Sbd

0.67 Ge

9 XTI saturation-current temp. exp - 3.0 3.0 jn

2.0 Sbd

10 FC coefficient for forward-bias - 0.5

depletion capacitance formula

11 BV reverse breakdown voltage V infinite 40.0

12 IBV current at breakdown voltage A 1.0E-3

**PROBLEM STATEMENT 1A**

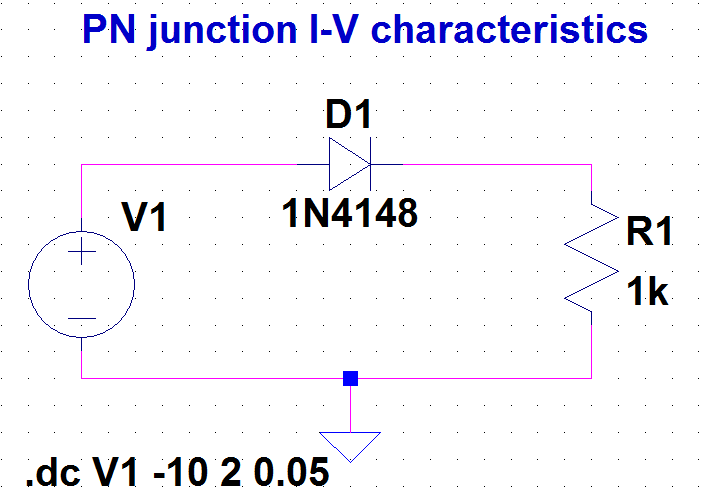
Simulate I-V characteristics for a pn junction diode (IN4148) using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 1A**

**SAMPLE CIRCUIT SCHEMATIC**

**This is the sreen shot of the schematic.**

**Strickly take the circuit capture as as shown here**



**For selection of white background in schematic or simulation waveform, follow these steps:**

**1. Go to simulate 2. Then control panel 3. Select waveforms 4. Then select color scheme 5. Then select schematic 5. (to makes wires black : select wires in selected item , then make color mix as all zero 6. To make background white : select background , then make color mix as 255.**

**For making the schematic circuit with thick lines, follows these steps:**

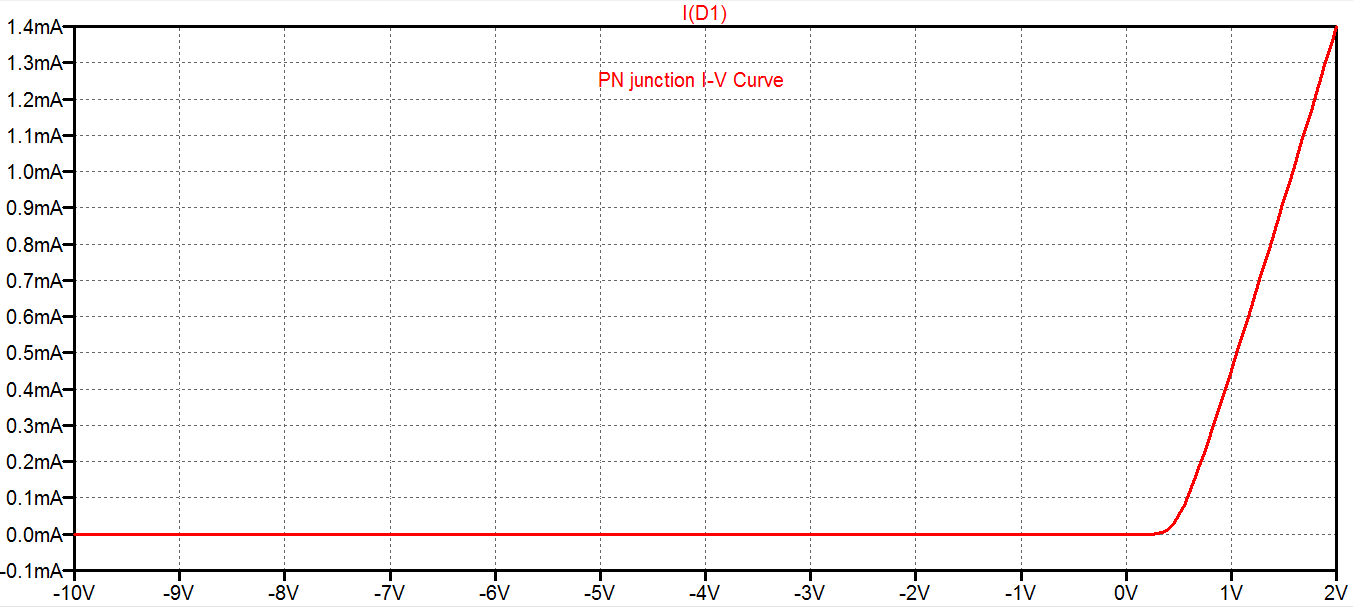
**1. Go to simulate 2. Then control panel 3. Drafting options 4. Put a tick on Draft with thick lines and also for text to be in bold, tick on bold.**

**SIMULATION RESULT 1A**

**SAMPLE SIMULATION RESULTS**

**This is the sreen shot of the simulation results**

**Strickly take the result plot as shown here**

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**For selection of white background in simulation waveform , follow these steps:**

**1. Go to tools 2. Then control panel 3. Select waveforms 4. To make background white : select background , then make color mix as 255.**

**For making waveform with bold lines, follow these steps:**

**1. Go to tools 2. Then control panel 3. Select waveform 4. Then tick on PLOT data with thick lines**

**For making the axis in waveforms dark in black, follow these steps:**

**1. Go to tools 2. Then control panel 3. Select waveforms 4. To make axis black : select Axis , then make color mix as zero.**

**Observe the following on the simulation plot for Problem Statement 1a**

1. Cut-in voltage : \_\_\_\_\_\_\_\_\_\_
2. Forward resistance : \_\_\_\_\_\_\_\_\_

**PROBLEM STATEMENT 1B**

Simulate I-V characteristics of a pn junction diode using SPICE programming in LTspice

**SPICE CODE 1B**

**SAMPLE spice code**

v1 1 0 dc

r1 2 0 1k

D1 1 2 myd

.model myd D(IS=5n)

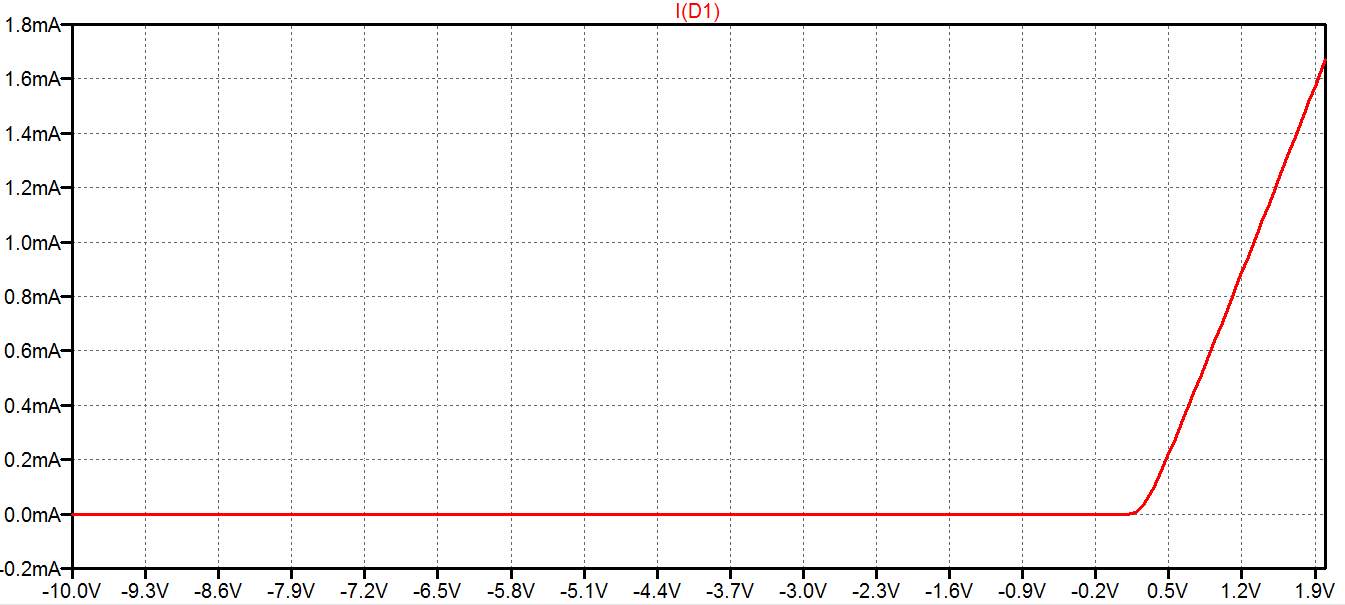
.dc v1 -10 2 0.05

**SIMULATION RESULT 1B**

**SAMPLE SIMULATION RESULTS**

**This is the sreen shot of the simulation results**

**Strickly take the result plot as shown here**

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**Observe the following on the simulation plot for Problem Statement 1b**

1. Cut-in voltage : \_\_\_\_\_\_\_\_\_\_
2. Forward resistance : \_\_\_\_\_\_\_\_\_

**PROBLEM STATEMENT 2A**

Simulate I-V characteristics for a zener diode (of breakdown voltage = 6.2 V) using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 2A**

**Attach here schematic of zener circuit**

**SIMULATION RESULT 2A**

**simulation results for zener will come here**

**Observe the following on the simulation plot for Problem Statement 2a**

1. Cut-in voltage : \_\_\_\_\_\_\_\_\_\_
2. Forward resistance : \_\_\_\_\_\_\_\_\_
3. Breakdown voltage : \_\_\_\_\_\_\_\_\_

**PROBLEM STATEMENT 2B**

Simulate I-V characteristics of a zener diode (of breakdown voltage = 6.2 V) using SPICE programming in LTspice

**SPICE CODE 2B**

**SAMPLE spice code**

**Hint: Only add breakdown voltage of 6.2V in code**

**SIMULATION RESULT 2B**

**simulation results for zener will come here**

**Observe the following on the simulation plot for Problem Statement 2b**

1. Cut-in voltage : \_\_\_\_\_\_\_\_\_\_
2. Forward resistance : \_\_\_\_\_\_\_\_\_
3. Breakdown voltage : \_\_\_\_\_\_\_\_\_

**PROBLEM STATEMENT 3A**

Simulate and calculate line regulation for zener diode (of breakdown voltage = 6.2 V) as voltage regulator using schematic capture in LTspice.

**CIRCUIT SCHEMATIC 3A**

**Attach here schematic of zener circuit**

**SIMULATION RESULT 3A**

**simulation results for zener will come here**

**Observe the following on the simulation plot for Problem Statement 3a**

1. % Line regulation : \_\_\_\_\_\_\_\_\_\_

**PROBLEM STATEMENT 3B**

Simulate and calculate line regulation for zener diode (of breakdown voltage = 6.2 V) as voltage regulator using SPICE programming in LTspice

**SPICE CODE 3B**

**SAMPLE spice code**

**Hint: Only add breakdown voltage of 6.2V in code**

**SIMULATION RESULT 3B**

**simulation results for zener will come here**

**Observe the following on the simulation plot for Problem Statement 3b**

1. % Line regulation : \_\_\_\_\_\_\_\_\_\_

**CONCLUSION:**